forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening, said forming the second layer including:

providing the shower head at a second distance from the substrate, the second distance lower than the first distance, and

providing through the shower head constituents forming the second layer.

B5 cont'd

REMARKS

Claims 1-31 are pending in this application. Claims 1-31 stand rejected. Claims 1, 14, 19, 26-29, and 31 have been amended. Applicant respectfully traverses the rejections for the reasons expressed herein below.

Enclosed with this Response is a marked-up version showing changes made to the specification by the present amendment; deletions are shown in brackets, while additions are underlined. The enclosed pages are captioned "Version With Markings to Show Changes Made".

Rejection under 35 U.S.C. § 103(a)

A. Prior Art Figure 9 and Chou

Claims 1-5, 14, and 16-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prior Art Figure 9 in view of United States Patent No. 5,861,345, issued to Chou et al. ("Chou"). Applicant respectfully traverses this rejection and requests reconsideration of claims 1-5, 14, and 16-18.

All claims 1-31, as amended, recite a method of forming a dieletric layer wherein a first dieletric layer is formed in (or completely fills (claim 26)) an opening at a first deposition rate, and a second dielectric layer is formed thereover at a second deposition rate greater than the first deposition rate. Support for this amendment can be found in the specification, for example, at page 6, lines 8-22, and in the claims. In particular, independent claims 1 and 14, and the claims that depend therefrom, recite a method of forming a dielectric layer in an opening comprising forming a first dielectric in the opening with an aspect ratio greater than about two. The first dielectric layer is formed at a first deposition rate in the opening wherein a portion of the opening not filled with the first layer has an aspect ratio of not greater than about two. A second dielectric layer is formed at a second deposition rate greater than the first deposition rate over the first layer wherein the second layer has a top surface that is not within the opening.

As stated on page 6, lines 10-14, a problem exists in the art in that openings having aspect ratios greater than about two are difficult to fill at relatively high deposition rates and often suffer from shadowing effects. The present invention solves this particular problem because it provides good gap-fill characteristics, even at high aspect ratios of greater than about two. In particular, it has been found that the first dielectric layer may be formed at a relatively low deposition rate, when the impingement rate is low, so that voids between the structures, due to the shadowing effect, are either eliminated or greatly reduced. As a result, the first dielectric layer provides improved protective, insulating and capacitive qualities in the critical gap areas or openings between the structures in order to protect the circuit from impurities, moisture, and stress related impacts.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the combination of prior art. MPEP §2143.03. In addition, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP §2143. Put another way, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination or modification. MPEP §2143.01. In addition, it must be remembered that a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. MPEP §2141.02.

As set forth in the disclosure at page 2, lines 7-11, Prior Art Figure 9 illustrates a dielectric formation problem known in the art as "shadowing", wherein some areas in the openings 118 between the structures 112 are more prone to developing voids 110 during the formation of the dielectric layer 102, thereby resulting in a less effective integrated circuit. As set forth in the disclosure, various attempts have been made to reduce or eliminate shadowing, and thereby improve the overall quality of the dielectric layer. The Prior Art Figure 9 represents a typical dielectric formation problem, and does not disclose a method wherein a first dielectric layer is formed in an opening at a first deposition rate and a second dielectric layer formed thereover at a second deposition rate greater than the first deposition rate, as recited in the claims. Rather, because of the shadowing effect, Prior Art Figure 9 illustrates a first dieletric layer that does not fill and is not formed in the opening. In addition, Prior Art Figure 9 provides no teaching wherein a second layer is formed at a second deposition rate greater than the first deposition rate. Prior Art Figure 9 provides no discussion on relative deposition rates or methods of providing methods of solving the "shadowing problem".

Furthermore, nothing in Chou, when combined with Prior Art Fig. 9, teaches or suggests the claimed invention. Chou teaches an *in situ* inter-dieletric process for forming multilevel metal structures. The process includes forming an SOG layer on an uneven semiconductor surface, treating a surface of the SOG layer with a plasma in a PECVD chamber, and forming a PECVD layer on the treated surface in the same PECVD chamber. Chou does not teach or suggest a method wherein a first dielectric layer is formed in an opening at a first deposition rate and a second dielectric layer is formed thereover at a second deposition rate greater than the first deposition rate. Indeed, the Examiner only cites Chou for the teaching of a method of forming a second dieleteric layer over a first dieletric layer, with the second layer having a top surface that is not within the opening.

It has been found that the assembly recited in the claims is effective for filling openings having an aspect ratio greater than about two. As set forth in the disclosure, and as previously discussed, openings having aspect ratios greater than two are difficult to fill at relatively high deposition rates and often suffer from shadowing. Neither Prior Art Figure 9 nor Chou, separately or in combination, disclose the method recited in claims 1-5, 14, and 16-18.

For at least the reasons discussed above that distinguish claims 1 and 14 of the present invention from the combined teachings of Prior Art Figure 9 and Chou, it is respectfully submitted that claims 1 and 14, and the claims that depend therefrom, are clearly distinguishable from the cited prior art and one not obvious in view thereof. Accordingly, withdrawal of the rejection to claims 1-5, 14, and 16-18 under 35 U.S.C. § 103(a) over Prior Art Figure 9 in view of Chou is respectfully requested.

B. Prior Art Figure 9 in view of Chou and further in view of Chakravarti

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Prior Art Figure 9 in view of Chou and further in view of Chakravarti. Applicant respectfully traverses this rejection and requests reconsideration of claim 15.

For at least the reasons set forth above, the Applicant asserts that claim 15, that depends from claim 14, is distinguishable from the combined teachings of Prior Art Figure 9 and Chou. In addition, nothing in Chakravarti, when combined with Figure 9 and Chou, teaches or suggests the claimed invention.

Chakravarti teaches a method of forming a memory device having a compact cell design with a deep trench storage capacitor self-aligned to a gate conductor cap insulator of the access transistor and connected by a buried strap. The method includes forming a dielectric masking layer having at least one opening, and, using the opening as a mask, forming the trench capacitor. Nothing in Chakravarti , alone or when combined with Figure 9 and Chan, discloses a method wherein a first dielectric layer is formed in an opening at a first deposition rate, and a second dielectric layer is formed thereover at a second deposition rate greater than the first deposition rate, as recited in claim 15. Indeed, the Examiner only cites Chakravarti for teaching a method of forming an opening in a substrate.

For at least the reasons discussed above, it is respectfully submitted that claim 15 is clearly distinguishable from the cited prior art. Accordingly, withdrawal of the rejection to claim 15 under 35 U.S.C. § 103(a) over Prior Art Figure 9 in view of Chou and Chakravarti is respectfully requested.

C. Prior Art Figure 9 in view of Chou and further in view of Lin

Claim 26 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Prior Art Figure 9 in view of Chou and further in view of U.S. Patent No. 5,969,409 issued to Lin. Applicant respectfully traverses this rejection and requests reconsideration of claim 26.

Lin discloses a wafer planarization process that combines chemical mechanical polishing and high density plasma enhanced chemical vapor deposition processes and employs a polishing stopper sub-layer embedded in an intermetal dielectric layer during the planarization of the intermetal dielectric layer.

The Applicant asserts that claim 26 is clearly distinguishable from the combined teachings of Prior Art Figure 9, Chou, and Lin. In particular, and as discussed above, the combined teachings of Figure 9 and Chou do not disclose or suggest a method wherein a first dielectric layer is formed in an opening at a first deposition rate and a second dielectric layer is formed thereover at a second deposition rate greater than the first deposition rate, as recited in claim 26. In addition, Lin provides no teaching that when combined with Figure 9 and Chou would render claim 26 obvious. Indeed, the Examiner cites Lin for the limited teaching of a dielectric layer completely filling an opening.

Accordingly, withdrawal of the rejection to claim 26 under 35 U.S.C. § 103(a) over Prior Art Figure 9 in view of Chou and Lin is respectfully requested.

D. Prior Art Figure 9 in view of Chou and further in view of Jang

Claims 6-13, 19-25, and 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prior Art Figure 9 in view of Chou and further in view of U.S. Patent No.

5,563,104 issued to Jang et al. ("Jang"). Applicant respectfully traverses this rejection and requests reconsideration of claims 6-13, 19-25, and 27-31.

Jang discloses a method of ozone-TEOS deposition using a two-step low and high temperature process. The dielectric layer is deposited in two steps. A first ozone-TEOS layer is deposited over the surfaces of the conducting layer at a first temperature to a first thickness. A second ozone-TEOS layer is deposited over the first layer at a second temperature to a second thickness wherein the second temperature is higher than the first temperature and the second thickness is greater than the first thickness, to complete the dielectric layer.

The Applicant asserts that claims 6-13, 19-25, and 27-31 are clearly distinguishable from the combined teachings of Prior Art Figure 9, Chou, and Jang. In particular, as discussed in detail above, the combined teachings of Figure 9 and Chou do not disclose or suggest a method wherein a first dielectric layer is formed in an opening at a first deposition rate and a second dielectric layer is formed thereover at a second deposition rate greater than the first deposition rate. In addition, Jang provides no teaching that when combined with Figure 9 and Chou would render claims 6-13, 19-25, and 27-31 obvious. Indeed, the Examiner cites Jang for the limited teaching of forming first and second dielectric layers through an ozone-TEOS deposition.

Also, the Applicant disagrees with the Examiner's assertion that it would be within the level of one of ordinary skill to form the first and second dieletric layers at first and second temperature, pressures, dopant concentrations, dopant flow rates, and shower head distances because the first and second dieletrc layers of Jang are different thickness which require different process settings, through the modification of the method of forming the dielectric layer of Prior Art Figure 9, the forming the second layer of Chou, and the forming of ozone-TEOS layers of Jang. It is respectfully submitted that in view of the distinctions set forth above between the

recited claims, as amended, and the teachings of Figure 9, Chou, and Jang, the Examiner's position is merely highsight reconstruction, and unsupported by the cited references.

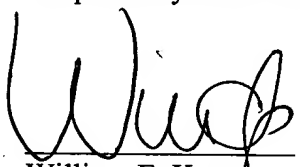
Accordingly, withdrawal of the rejection to claims 6-13, 19-25, and 27-31 under 35 U.S.C. § 103(a) over Prior Art Figure 9 in view of Chou and Jang is respectfully requested.

CONCLUSION

Applicant submits that claims 1-31 of the present invention recite a novel and non-obvious method of forming a dieletric layer. The cited references, neither alone or in combination, teach or suggest the claimed methods. In view of the foregoing, Applicant respectfully submits that the subject application is in condition for allowance. Accordingly, reconsideration of the rejections and allowance of the claims at an early date are earnestly solicited.

If the undersigned can be of assistance to the Examiner in addressing issues to advance the application to allowance, please contact the undersigned at the number set forth below.

Respectfully submitted,



William E. Kuss
Reg. No. 41,919

KIRKPATRICK & LOCKHART LLP
Henry W. Oliver Building
535 Smithfield Street
Pittsburgh, Pennsylvania 15222

Phone: (412) 355-6323
Fax: (412) 355-6501

Version With Markings to Show Changes Made

In the Claims:

Claims 1, 14, 19, 26-29, and 31 have been amended as follows:

1. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening at a first deposition rate, the opening having an aspect ratio greater than about two, and wherein a portion of the opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening.

14. (Amended) A method of forming a dielectric layer during the manufacture of a semiconductor device, comprising:

providing a substrate;

forming an opening relative to the substrate, the opening having an aspect ratio greater than about two;

forming a first dielectric layer in the opening at a first deposition rate, wherein a portion of the opening not filled with said first dielectric layer has an aspect ratio of not greater than about two; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening.

19. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening at a first deposition rate, the first layer having a first process setting; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening and having a second process setting at a predetermined relationship with the first process setting.

26. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer completely filling the opening at a first deposition rate, the opening having an aspect ratio greater than about two; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate.

27. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening at a first deposition rate, the first layer being formed at a first temperature; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening and being formed at a second temperature, the first temperature being greater than the second temperature.

28. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening at a first deposition rate, the first layer being formed at a first pressure; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening and being formed at a second pressure, the first pressure being greater than the second pressure.

29. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening at a first deposition rate, the first layer having a first dopant concentration; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening and having a second dopant concentration, the first dopant concentration being less than the second dopant concentration.

31. (Amended) A method of forming a dielectric layer in an opening, comprising:

forming a first dielectric layer in the opening at a first deposition rate, said forming the first layer including:

providing a shower head at a first distance from the substrate, and

providing through the shower head constituents forming the first layer; and

forming a second dielectric layer over the first dielectric layer at a second deposition rate greater than said first deposition rate, the second layer having a top surface that is not within the opening, said forming the second layer including:

providing the shower head at a second distance from the substrate, the second distance lower than the first distance, and

providing through the shower head constituents forming the second layer.